

Figure 1: prior art VHDL listing

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;

ENTITY test IS
    PORT(
        clk : IN std_logic;
        rst : IN std_logic;
        in1 : IN unsigned(7 downto 0);
        in2 : IN unsigned(7 downto 0);
        out1 : OUT unsigned(7 downto 0)
    );
END;

ARCHITECTURE behavioral OF test IS
BEGIN
    main : PROCESS
        VARIABLE min1 : unsigned(7 downto 0);
        VARIABLE min2 : unsigned(7 downto 0);
    BEGIN
        WAIT UNTIL (clk'EVENT and clk = '1');
        min1 := in1;
        min2 := in2;
        loop1 : WHILE ( min1 < min2 ) LOOP
            IF (min2 > 0) THEN
                FOR x IN 0 TO 7 LOOP
                    min1 := min1 + min2;
                    min2 := min2 - 1;
                END LOOP;
            ELSE
                FOR x IN 10 DOWNTO 5 LOOP
                    min1 := min1 - x;
                END LOOP;
            END IF;
        END LOOP;
        out1 <= min1 * min2;
    END PROCESS;
END;
```

Annotations in the original image:

- Arrow 100 points to the `USE ieee.std_logic_arith.ALL;` line.
- Arrow 110 points to the `loop1 : WHILE` line.
- Arrow 120 points to the `IF (min2 > 0)` line.
- Arrow 130 points to the `FOR x IN 0 TO 7` line.
- Arrow 140 points to the `FOR x IN 10 DOWNTO 5` line.

Figure 2a: prior art Gantt chart

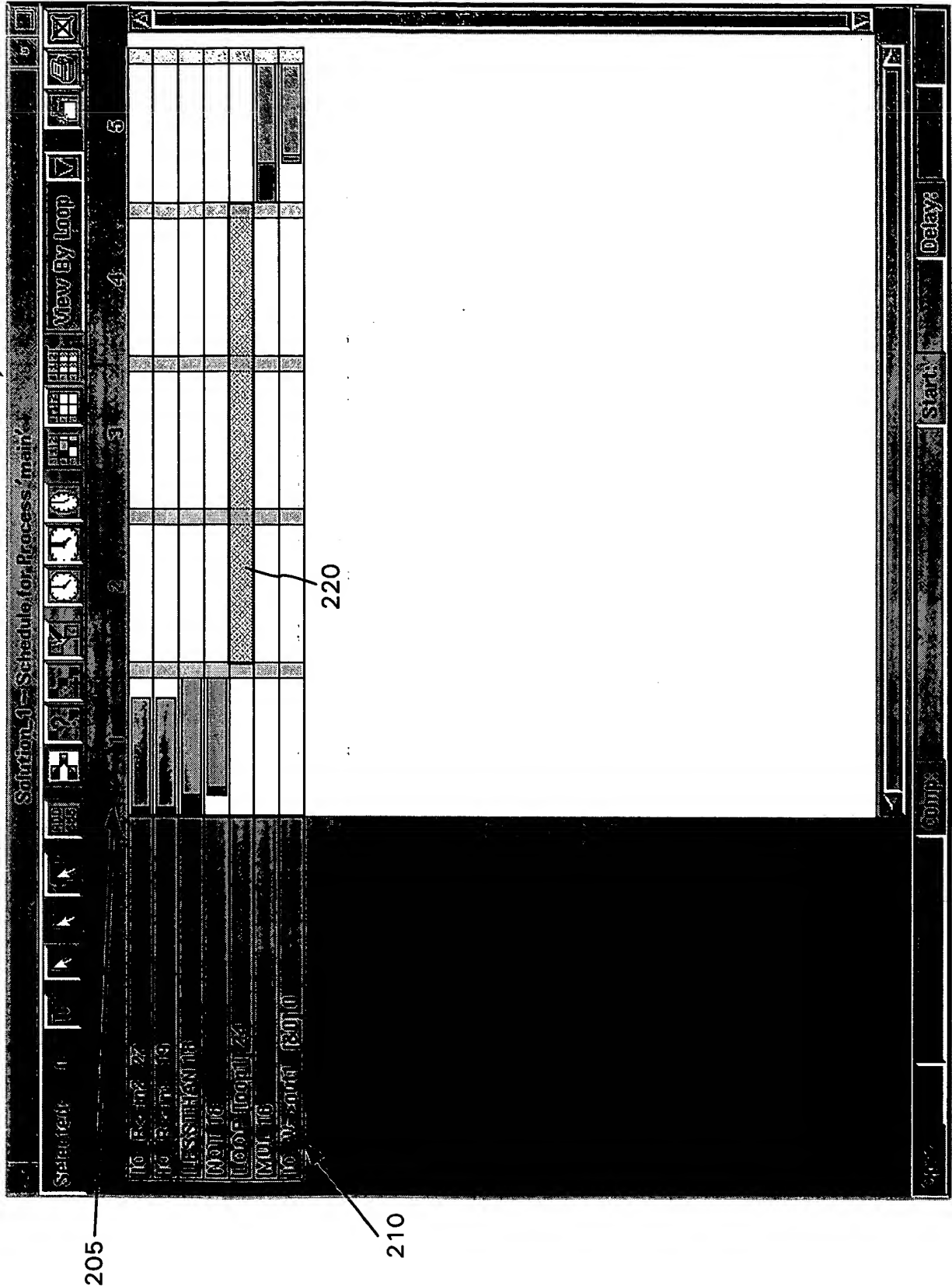


Figure 2b: prior art Gantt chart

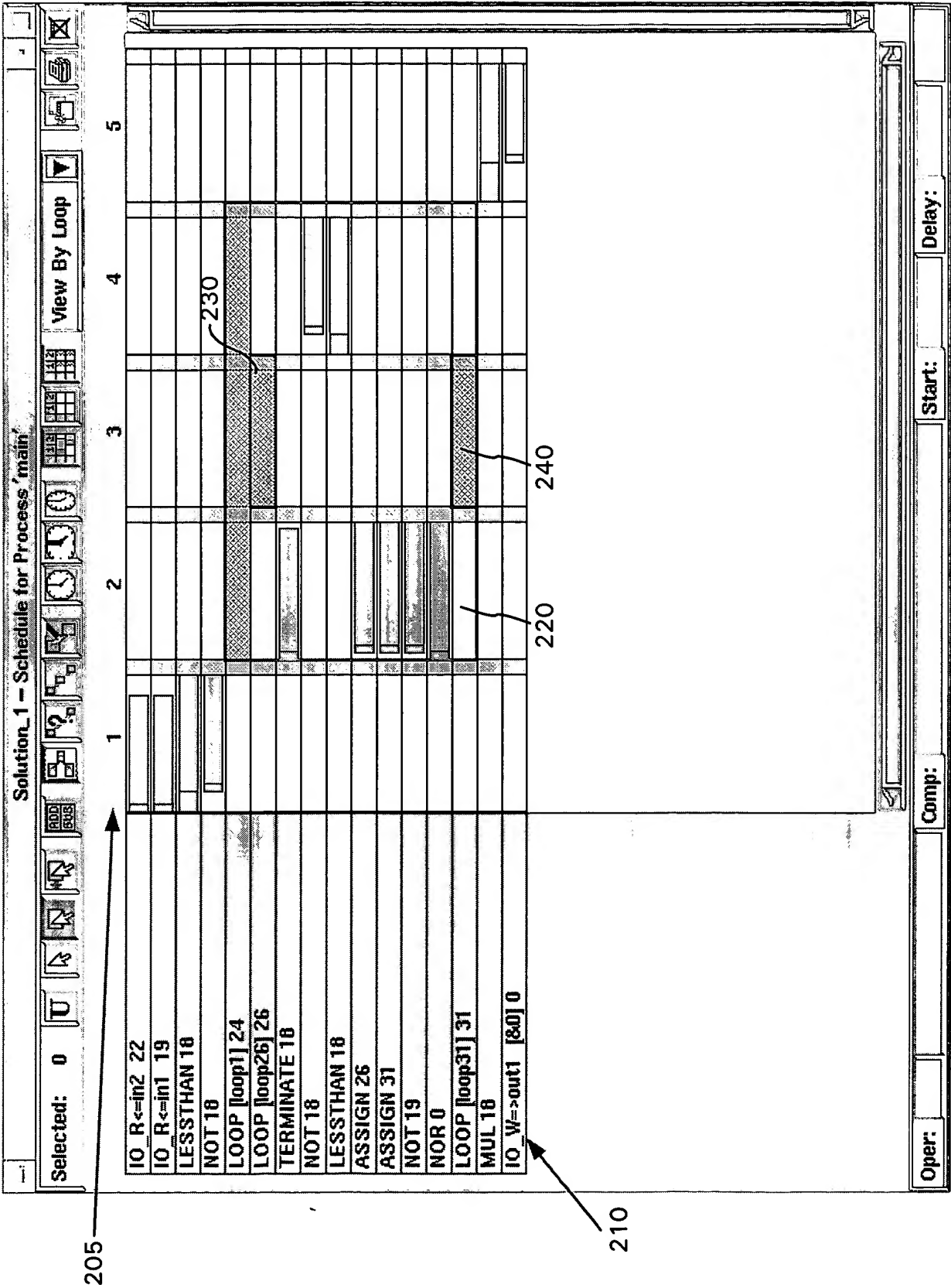


Figure 2c: prior art Gantt chart

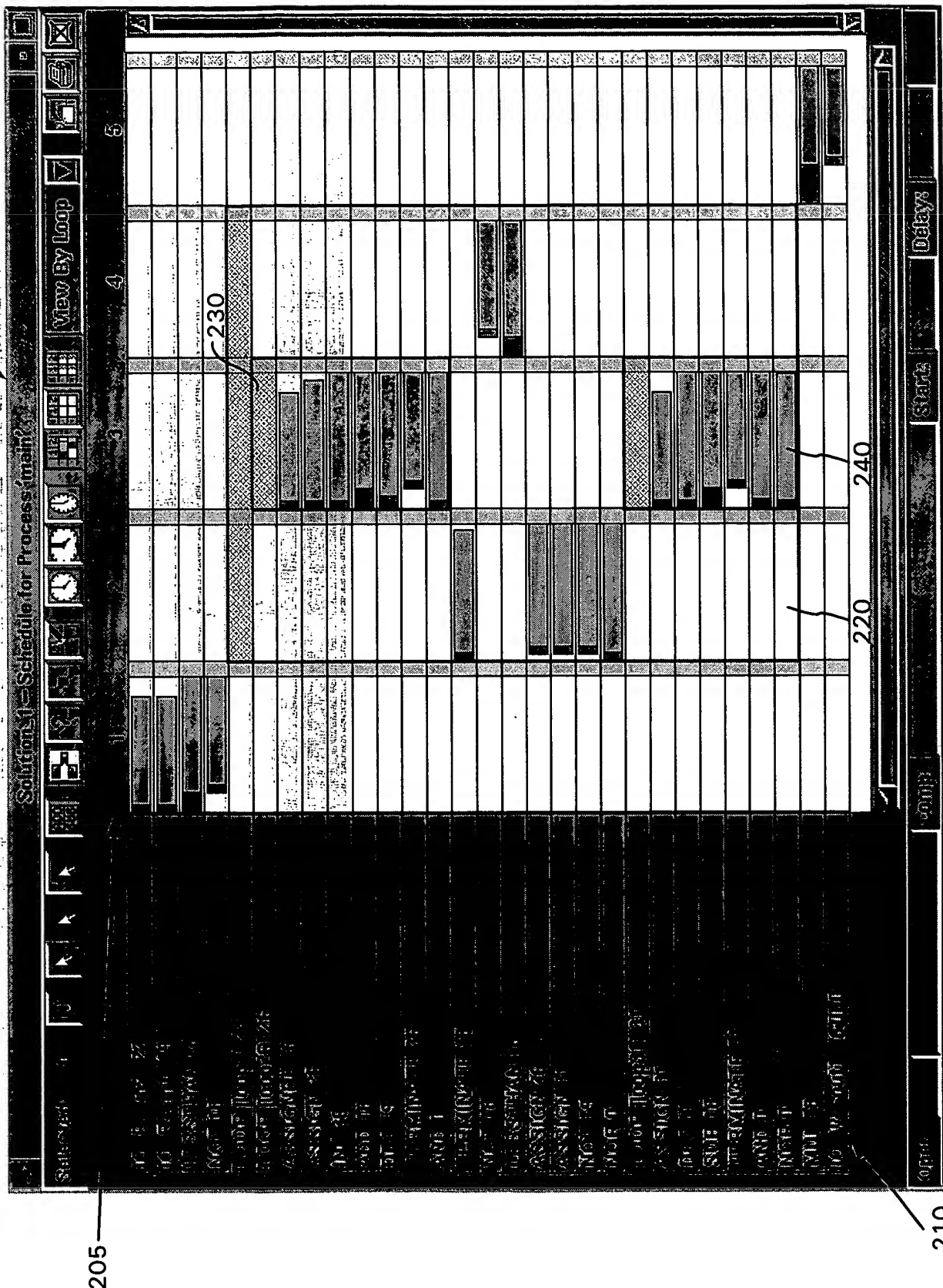


Figure 3

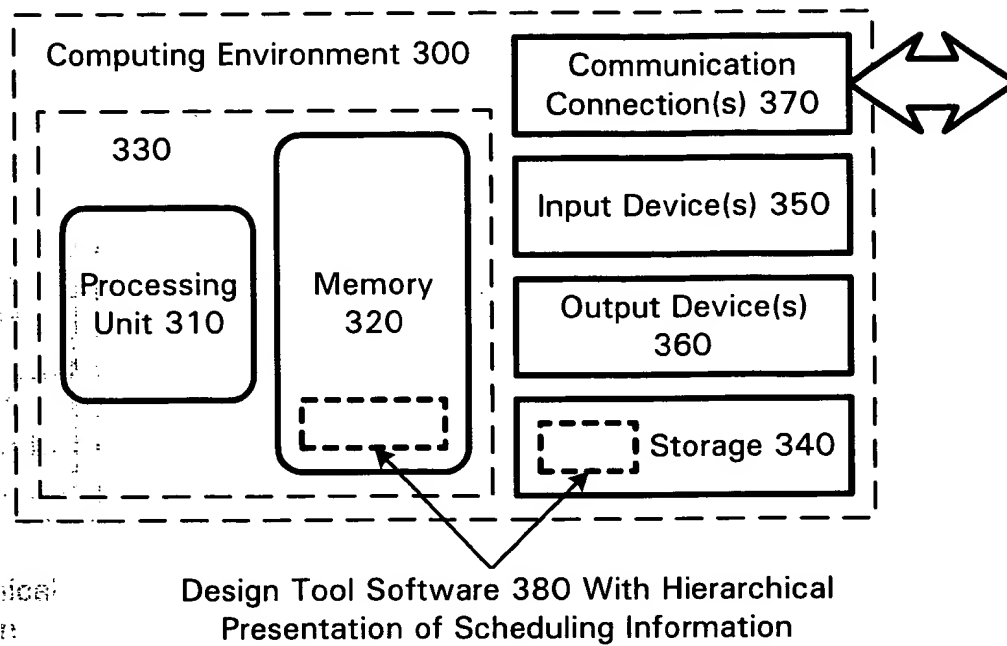


Figure 4

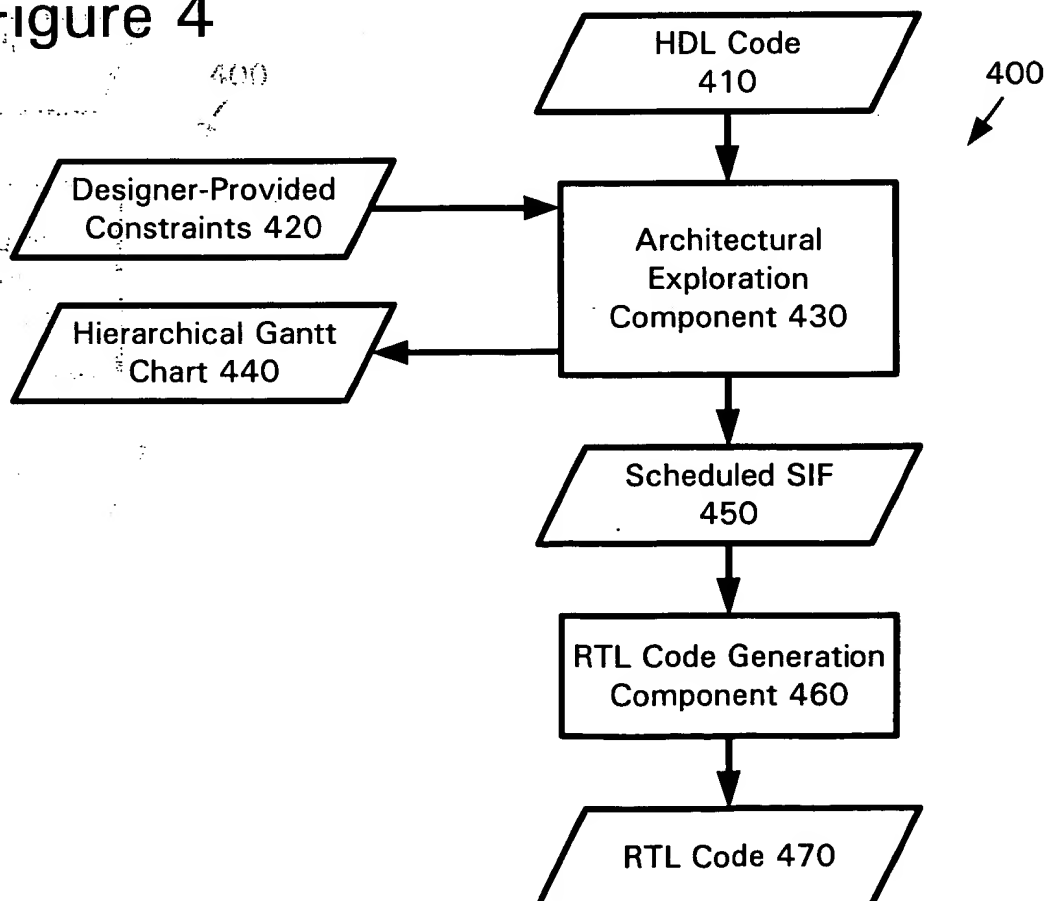


Figure 5

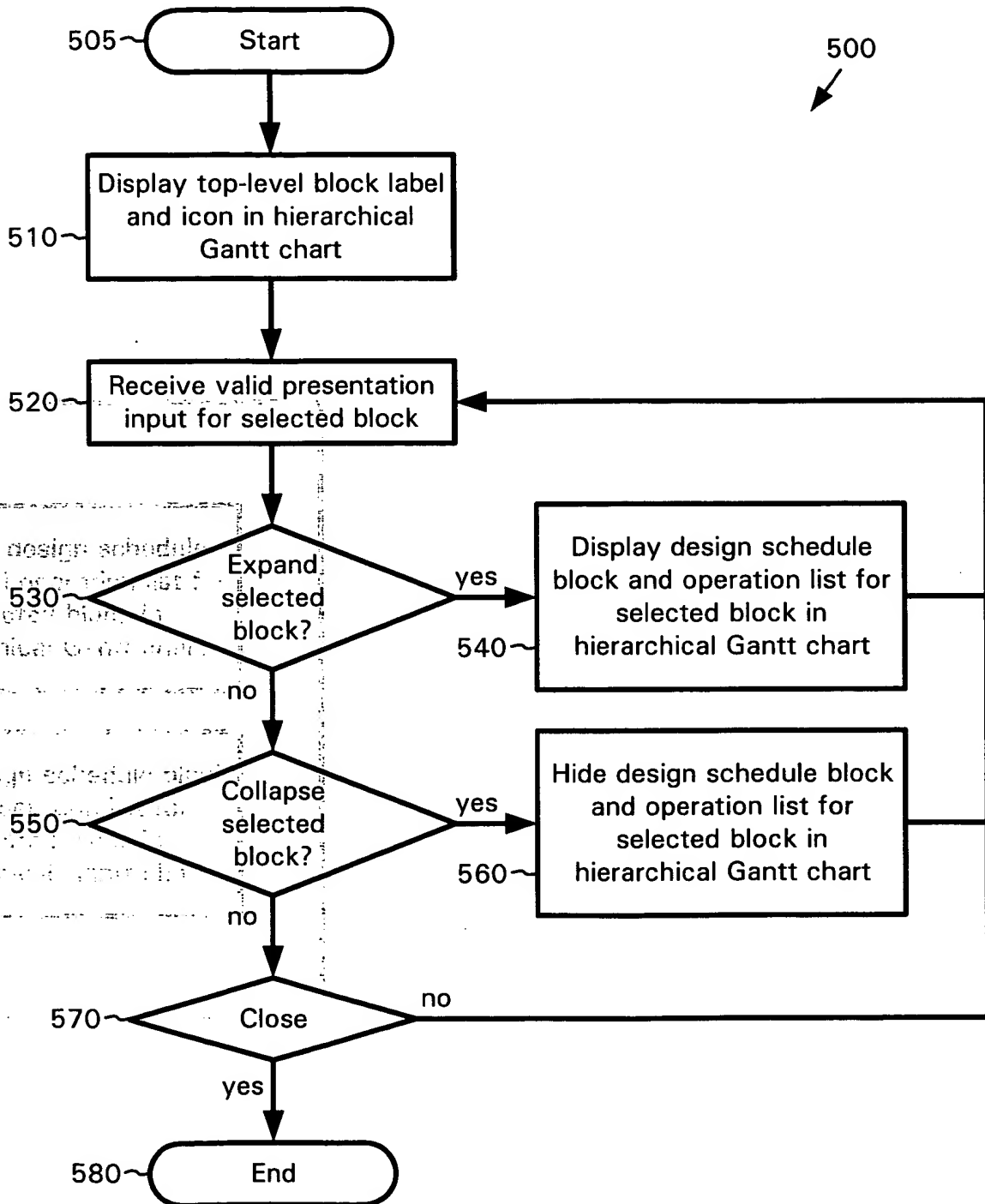


Figure 6a

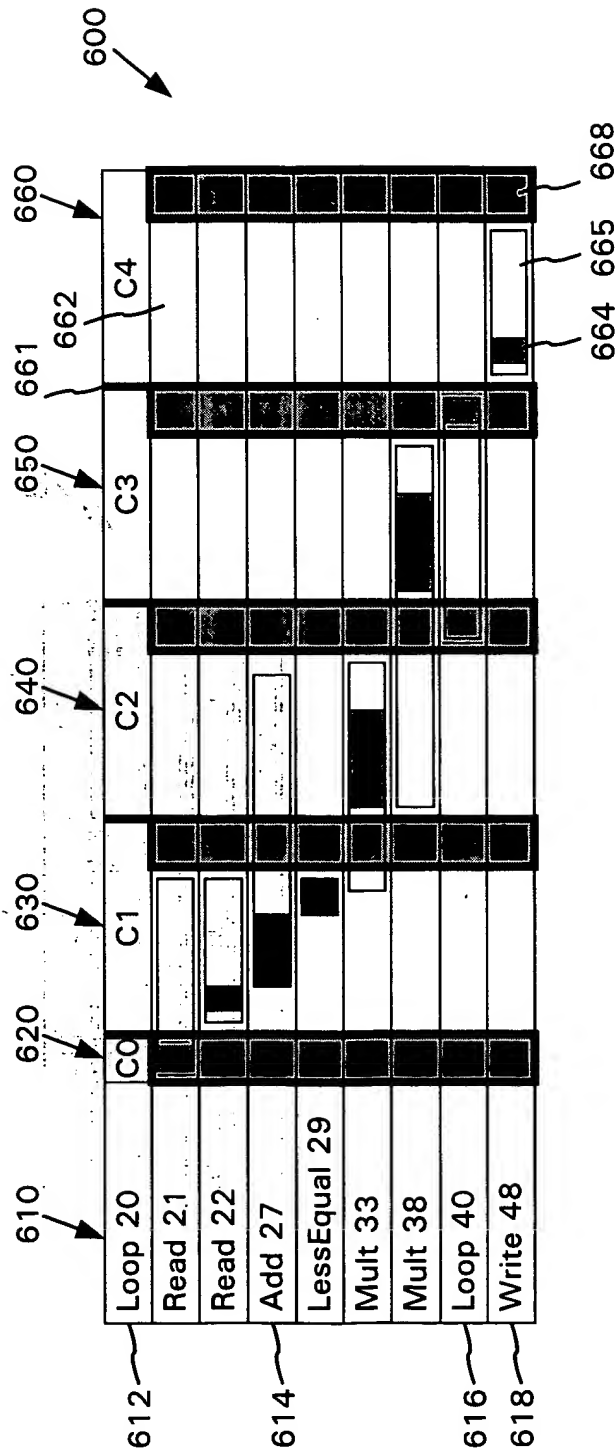


Figure 6b

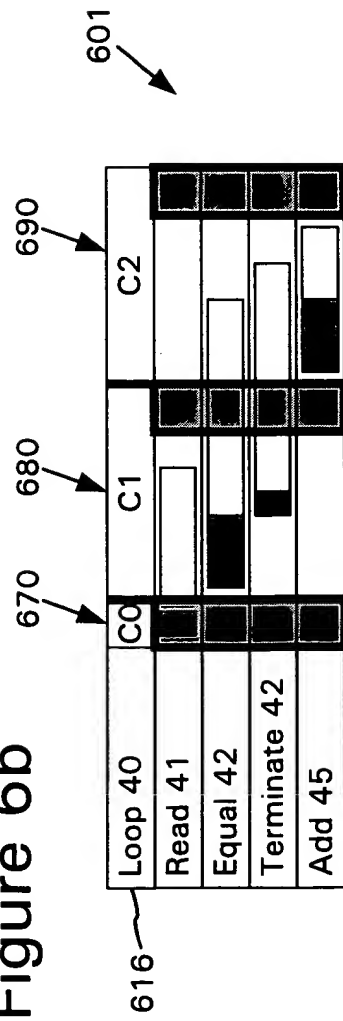


Figure 6c

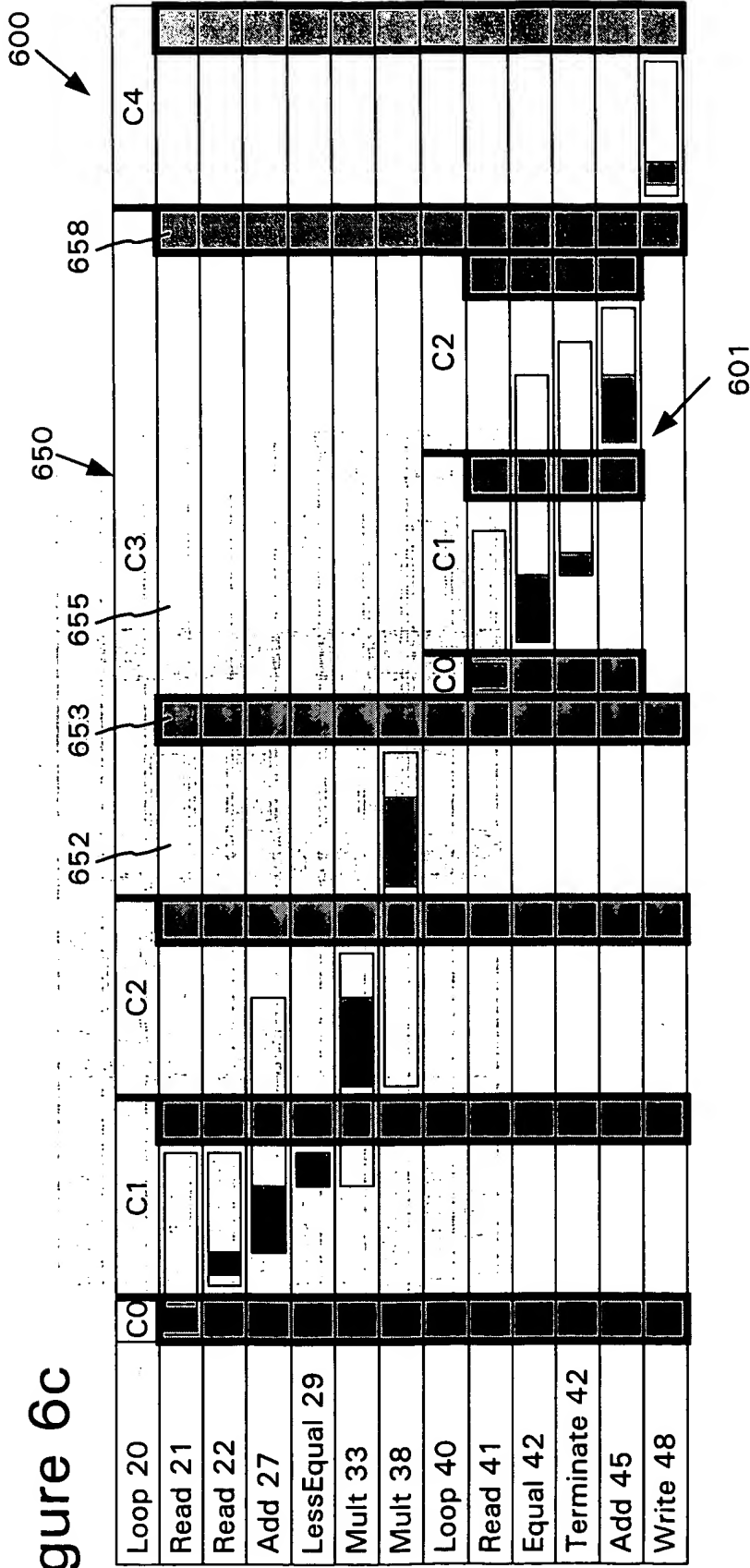


Figure 6d

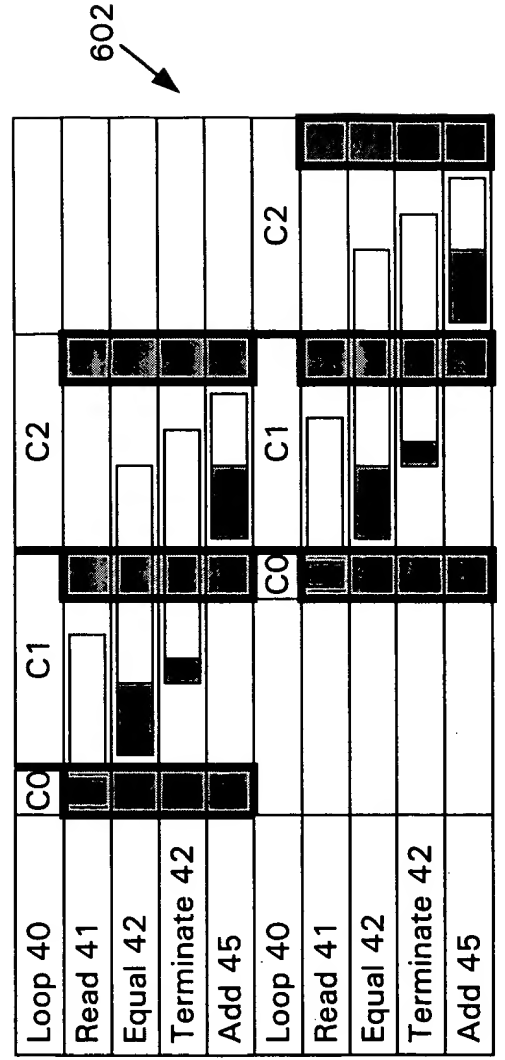




Figure 7b

700

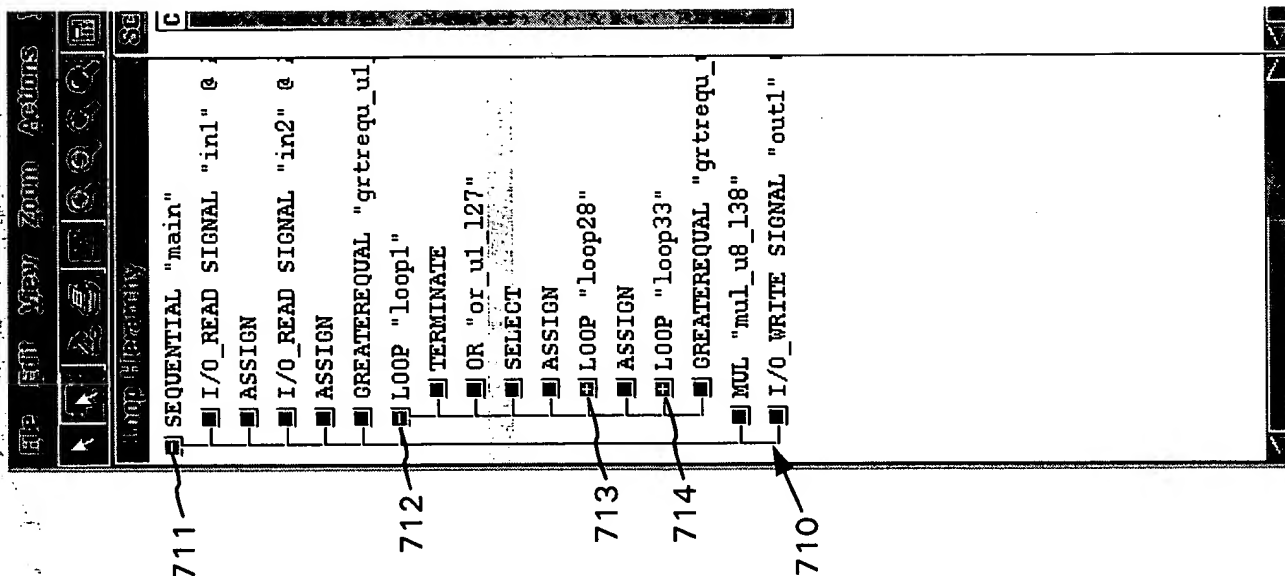
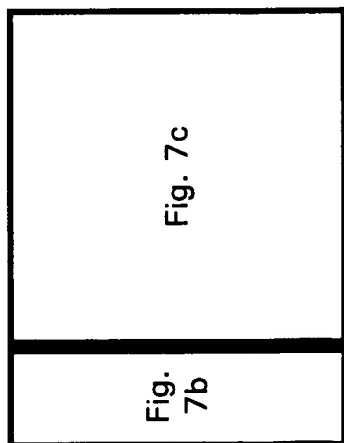
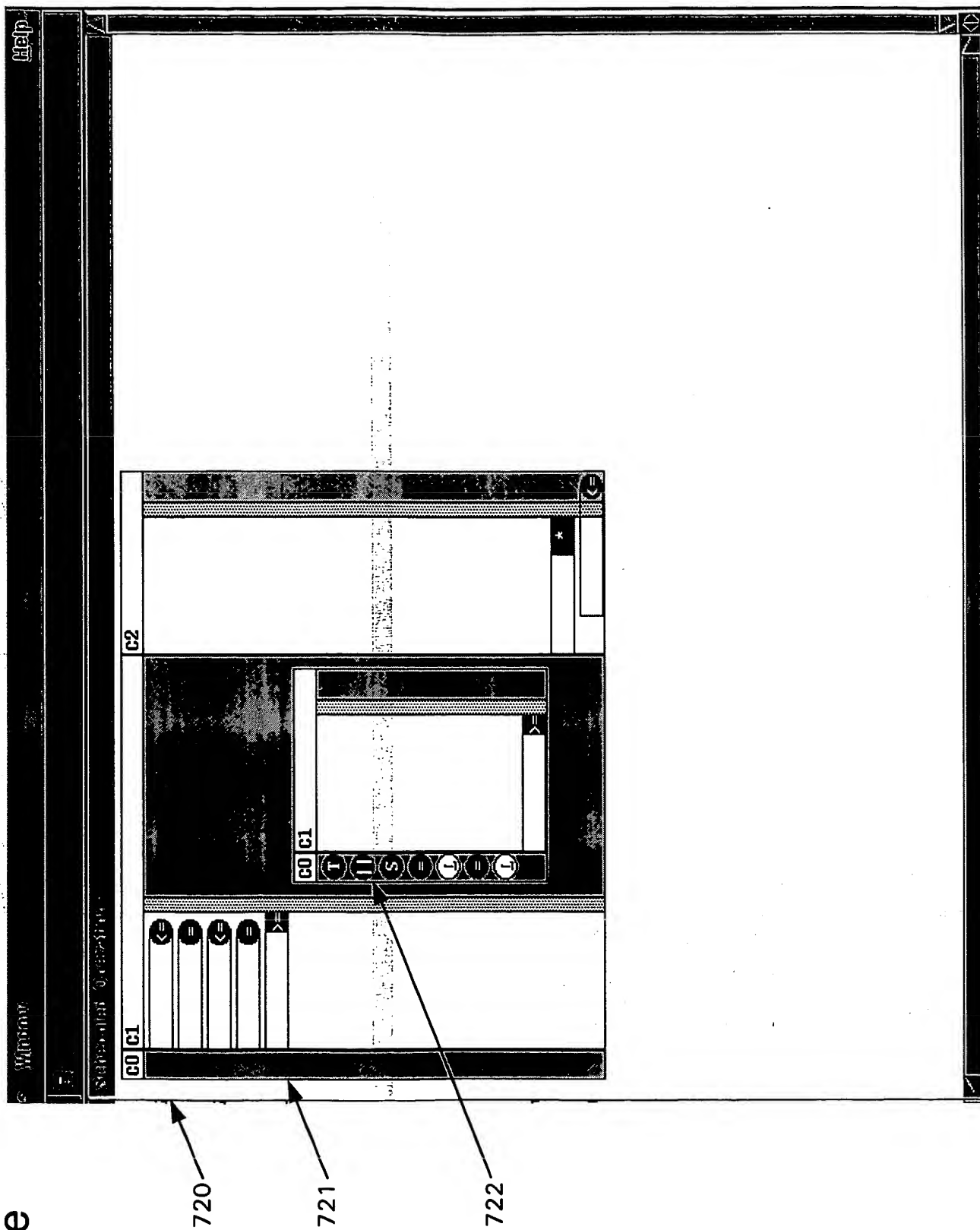


Figure
7c



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Figure 7d

700

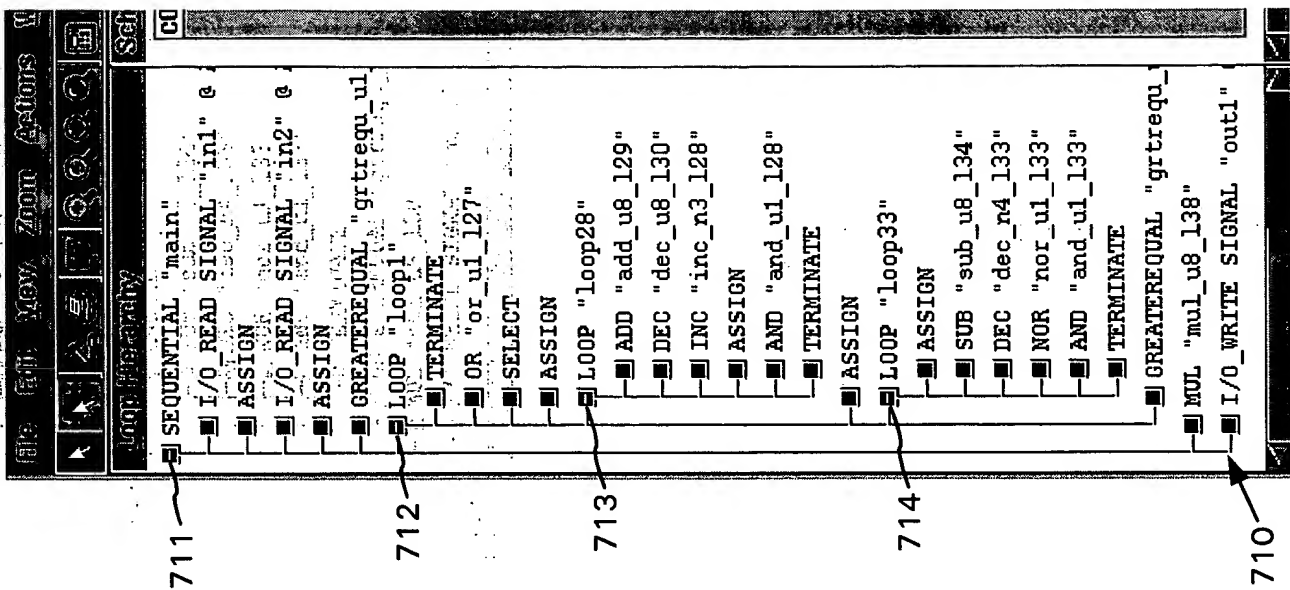
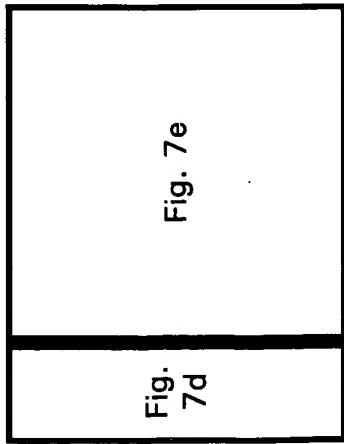


Figure
7e

